SFP+ Loopback Adapter

Features and Benefits

- SFP+ MSA Compliant
- Data rates to 12 Gbps
- Hot Pluggable
- Operates on 3.3V supply
- Serial ID
- Mates with 20 pos SMT

Applications

- Telecommunication
- Networking
- Switches
- Data Communication

Reference Information

- Form Factor: SFP+
- Housing: Die Cast
- Host Connector
  - Molex p/n 74441
- SFP+ EMI Cage
  - Molex p/n 74737

Sales Drawing

- SD-xxxxx-xxxx

SFP+ Loopback Adapter

SFP+ General Overview

The SFP+ Loopback Module is a high performance integrated duplex serial data link for loopback communications. The loopback supports data rates of up to 12 Gbps. Applications include Fibre Channel, InfiniBand, and Gigabit Ethernet. The hot pluggable feature allows changing to/from another SFP+ compatible module without having to remove system power. Each module provides serial ID compliance.

SFP+ Loopback Options

The SFP+ Loopback Module is available as a universal loopback only at this time.

- The standard loopback was designed to test the signal integrity of the host's high speed communications.
- The universal loopback module adds an I2C port expander, and power supply load resistors to the standard loopback. The I2C port expander enables the host to test the functionality of all low speed I/O while the power supply load resistors stresses the DC supplies sources.

SFP+ Ordering Information

Part Numbe	Options
74765-0906	• Universal Loopback Adapter o 0 dB High Speed Signal Attenuation o 8-bit I2C Port Expander for Low Speed Signaling o 50 uinches gold o Thumb-Latch Backshe lls

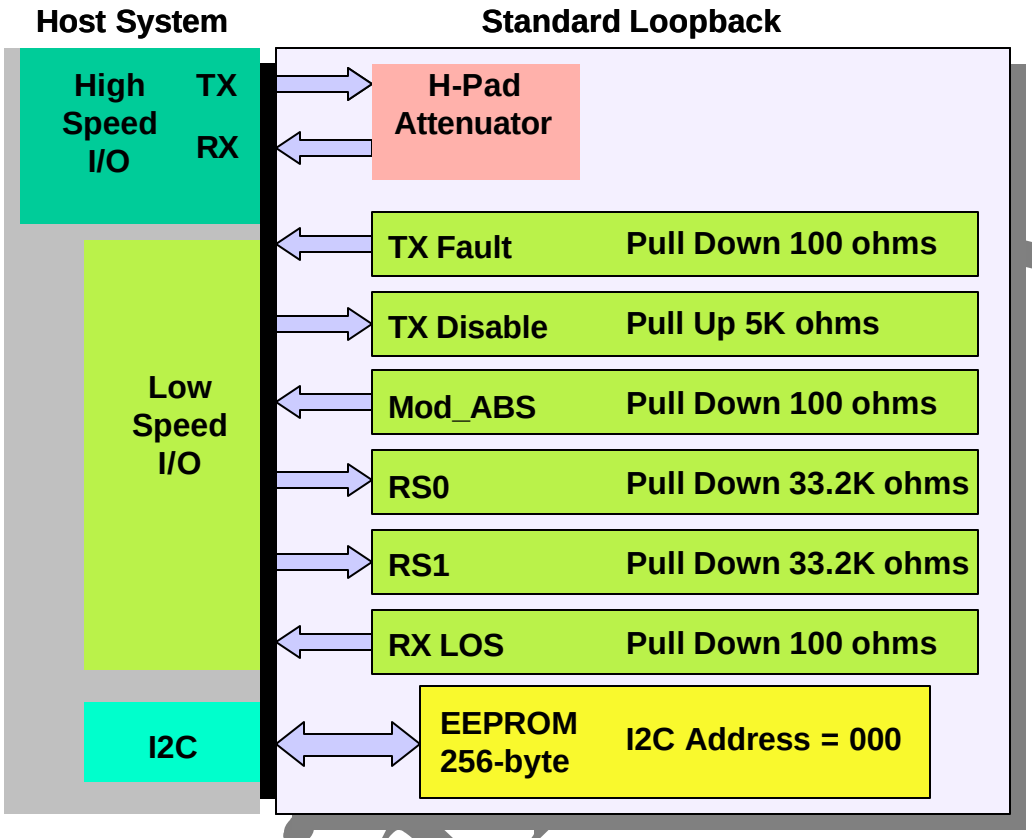
Loopback Performance Specifications

MODULE SPECIFICATIONS - RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNITS	NOTES
Storage Temperature	-40		85	ºC	
Ambient Operating Temperature	0		70	ºC	
Data DC Voltage	-10		10	Vpk	V (Tx+,Tx-,Rx+, Rx-) to ground
Supply Voltage	3.1	3.3	3.47	Vdc	
Supply Current (loopback only)		2	30	mA	
Supply Current (universal power loading)	266	280	294	mA	

Data Path					
Baud Rate			12	Gbps	
Bit Error Rate			1E-12		Errors/Bit
Impedance			100	ohms	Differential, DC coupled

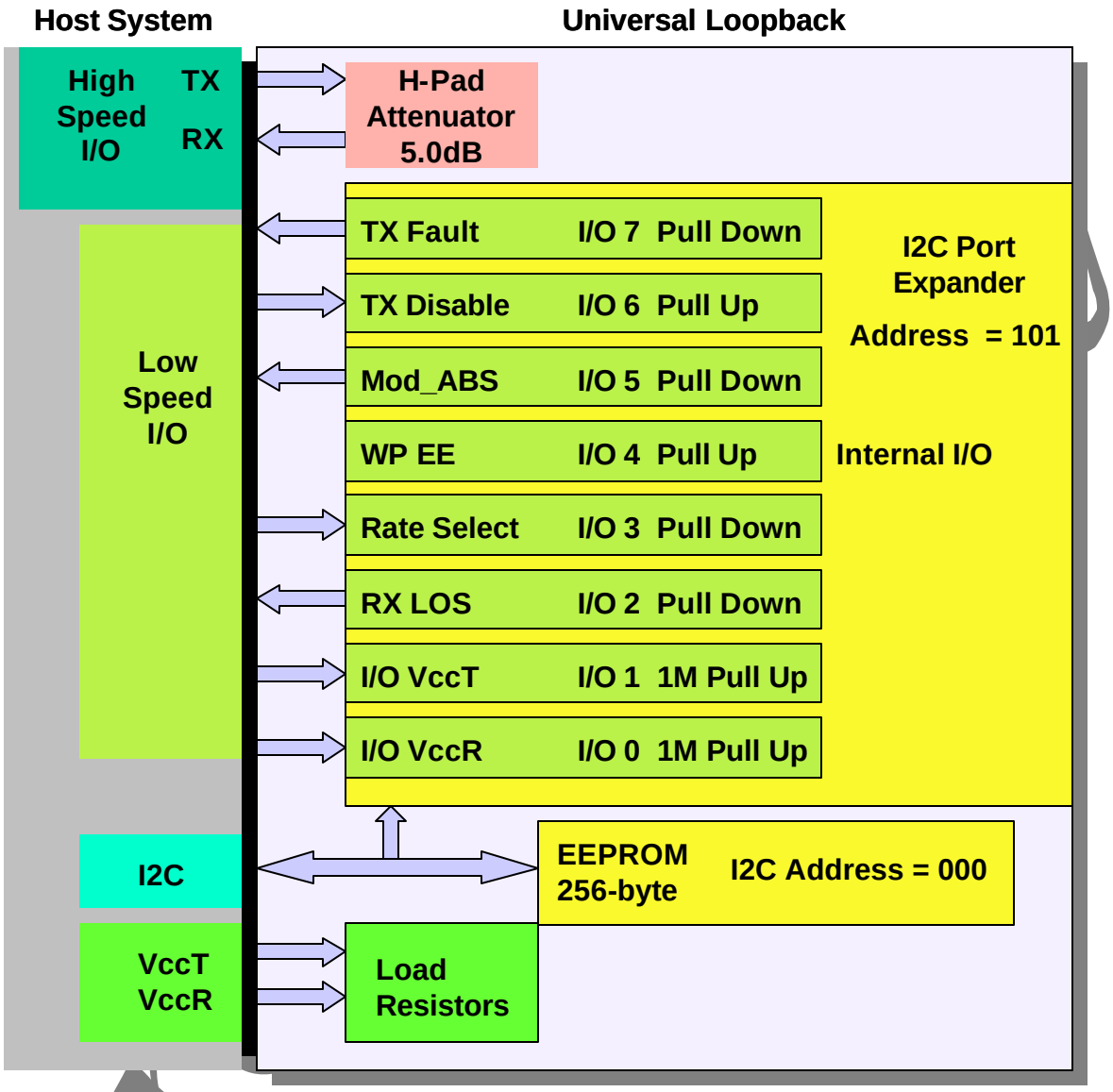
Standard Loopback Block Diagram



SFP+ Standard Loopback Serial ID

The 256-byte two-wire EEPROM is write protected on SFP+ Standard Loopback Module.

Block Diagram with 8-bit I2C Port Expander for Low Speed Signaling



SFP+ Universal Loopback Serial ID

The 256-byte two-wire EEPROM is write protected on SFP+ Universal Loopback Module.

Printed Circuit Board Hose Connector Mating

Molex's SFP+ Loopback Adapter (p/n series 74765) contains a 0.039 inch thick printed circuit board that mates with the 20 position SMT host connector (Molex p/n 74441-0001) which complies with the SFP+ MSA recommended mating sequence. The printed circuit board pads were designed for a sequenced mating of:

- First mate – ground contacts
- Second mate – power contacts
- Third mate – signal contacts

The electrical pad layout is illustrated in Figure 1. Typical contact pad plating for the printed circuit board is 0.38 micrometers minimum hard gold over 1.27 micrometers minimum thick nickel. A diagram of the host connector is show in Figure 2. Signal inputs/outputs on the SFP+ transceiver modules from the 20-pin host connector are AC coupled and internally terminated to 100 ohms differential (TD+, TD-, RD+, RD-).

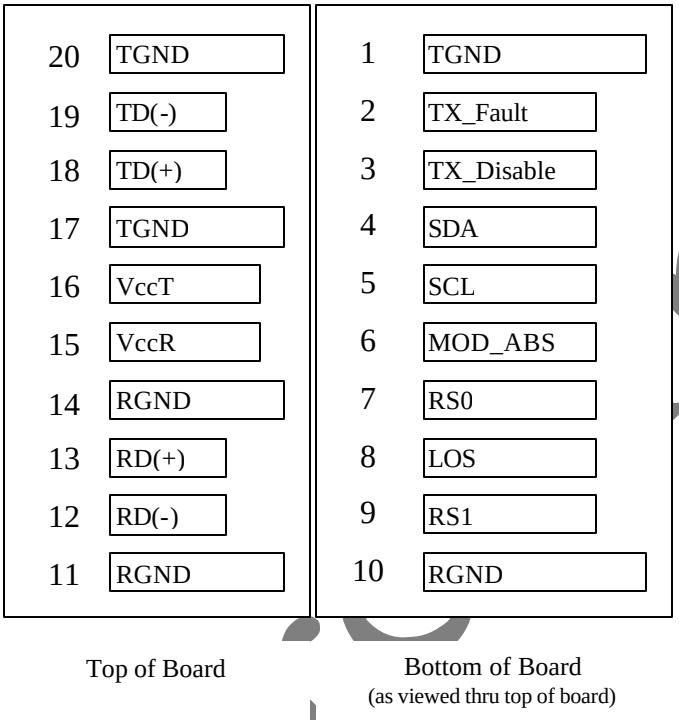


Figure 1. SFP+ Transceiver Electrical Pad Layout

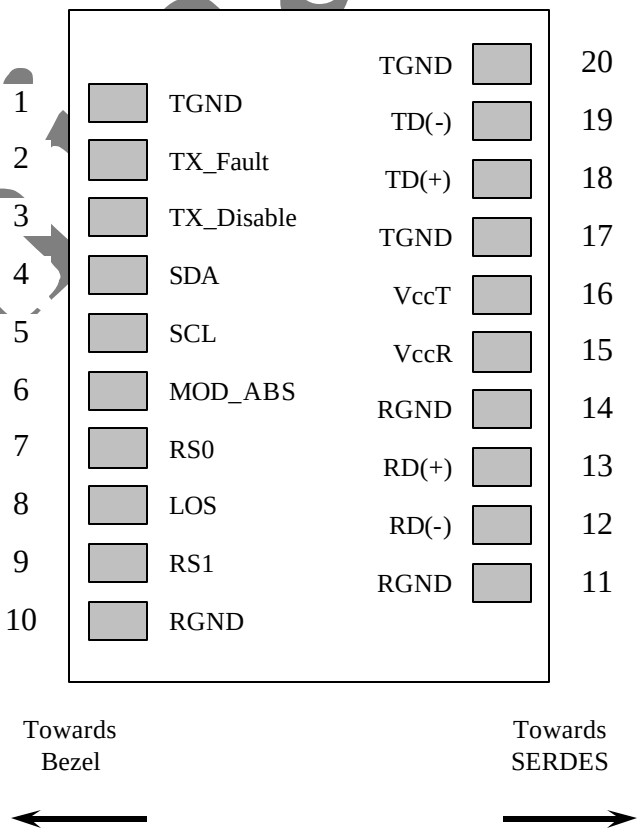


Figure 2. Diagram of the Host Board Connector Block Pin Number and Names

Power Supply Filtering Network

Recommended Power Supply Filtering Network

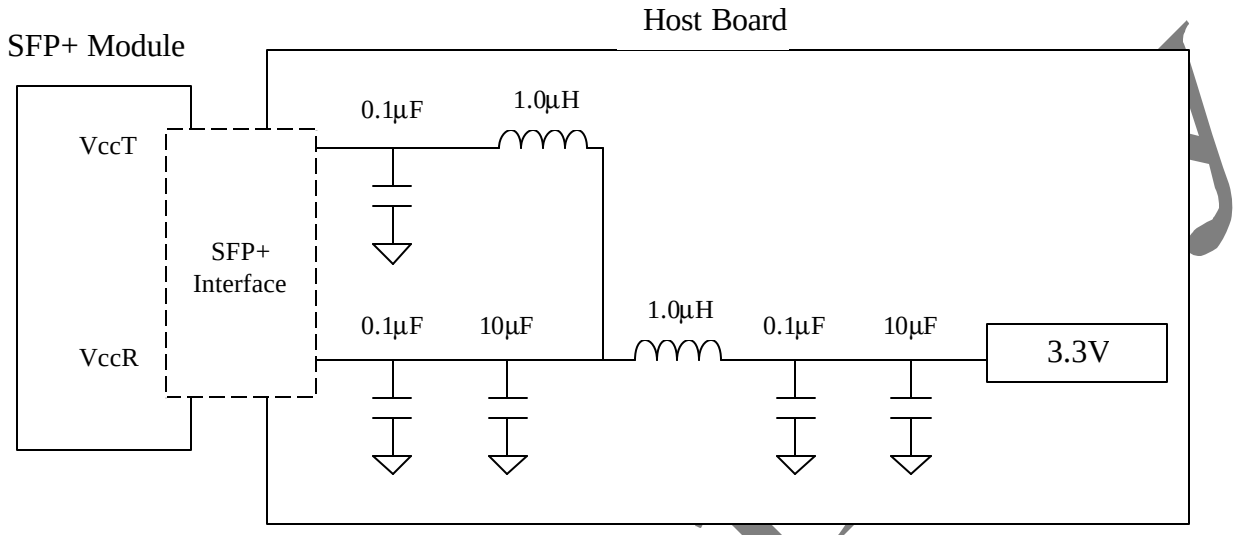


Figure 3. Recommended Host Board Supply Filtering Network

SFP+ AC Coupling

The SFP+ loopback high speed signals are internally AC coupled and terminated to 100 ohms.

Passive Electrical Interface – Pin Descriptions – Standard Loopback

Pin	Name	Description
PIN 1	TGND	Transmit ground
PIN 2	TX_FAULT	Internally tied to Transmit ground. TX_FAULT is not implemented.
PIN 3	TX_DISABLE	Internally pulled up to Vcc through a 5.11k ohm resistor. TX_DISABLE is not implemented.
PIN 4	SDA	Signal SDA (Data) of the 2-wire serial ID interface
PIN 5	SCL	Signal SCL (Clock) of the 2-wire serial ID interface
PIN 6	MOD_ABS	This pin is internally tied to Transmit ground
PIN 7	RS0	Pin is internally pulled low through a 33.2k resistor. Rate Select is not implemented.
PIN 8	LOS	Internally tied to Receiver Ground. LOS is not implemented.
PIN 9	RS1	Pin is internally pulled low through a 33.2k resistor. Rate Select is not implemented.
PIN 10	RGND	Receiver ground
PIN 11	RGND	Receiver ground
PIN 12	RD-	Differential receiver outputs. User to terminate to 100 ohms differential at SERDES.
PIN 13	RD+	Differential receiver outputs. User to terminate to 100 ohms differential at SERDES.
PIN 14	RGND	Receiver ground
PIN 15	VCCR	Receive power
PIN 16	VCCT	EEPROM power
PIN 17	TGND	Transmit ground
PIN 18	TD+	Differential transmitter inputs. Internally terminated to 100 ohms differential.
PIN 19	TD-	Differential transmitter inputs. Internally terminated to 100 ohms differential.
PIN 20	TGND	Transmit ground

Universal Loopback - I2C Port Expander Communications

The Philips PCA9557PW is an 8-bit parallel input/output port expander controlled over the I2C serial communications link. The port expander is open drain and contains registers for input, input polarity, output, and input/output configuration. I2C communications is similar to the serial ID EEPROM.

At power-on reset, all registers on the PCA9557PW return to their default states. All I/O pins default to inputs on reset or power-up.

I2C Control Byte for Port Expander:

Slave Address							
0	0	1	1	A2	A1	A0	R/W
Fixed				Programmable			

Control Register (Command Byte):

The control register is used to specify which I/O register is active.

0	0	0	0	0	0	D1	D0

D1	D0	Name	Type	Function
0	0	Register 0	Read	Input port register
0	1	Register 1	Read/Write	Output port register
1	0	Register 2	Read/Write	Polarity inversion register
1	1	Register 3	Read/Write	Input / Output configuration register

Input Register 0:

The input register is read-only. This register contains the logic level of the port expander's input or output pins.

I7	I6	I5	I4	I3	I2	I1	I0

Output Register 1:

The output register is used to set the logic level of output pins. An input pin is not effected by setting the bit in the output register.

Bit	O7	O6	O5	O4	O3	O2	O1	O0
Default	0	0	0	0	0	0	0	0

Polarity Register 2:

The polarity register sets the polarity inversion of the input pins. A zero written into the register will maintain the input pin's polarity.

Bit	N7	N6	N5	N4	N3	N2	N1	N0
Default	1	1	1	1	0	0	0	0

Configuration Register 3:

The configuration register sets the pin's direction to input or output. A zero written into the register will set the pin to an output. A one written into the register will set the pin to an input.

At power-up reset, the I/O pins will default to inputs.

Bit	C7	C6	C5	C4	C3	C2	C1	C0
Default	1	1	1	1	1	1	1	1

Reads / Writes

Reading and writing to the I2C port expander is similar to reading and writing to the serial EEPROMs. For a random read, the host issues a start, write control byte, sets the register address, issues a restart, read control byte, read the data. A random write is started with a start, write control byte, setting of the register address, and then writes the data.

Random Read

	Slave Address									Command Byte								
Start	0	0	1	1	A2	A1	A0	0	ACK	0	0	0	0	0	0	D1	D0	ACK
								Write										

	Slave Address									Read Data	
Restart	0	0	1	1	A2	A1	A0	1	ACK	Data	Stop
								Read			

Random Write

	Slave Address									Command Byte								
Start	0	0	1	1	A2	A1	A0	0	ACK	0	0	0	0	0	0	D1	D0	ACK
								Write										

Write Data		
Data	ACK	Stop

Power-On I2C Port Expander Sequence

After a power-on-reset, the I2C port expander configuration and polarity must be initialized. Random writes were used to initialize the port expander.

The power-on sequence is as follows.

1. Set Configuration Register

Bus Address	0x05
Command Byte	0x03
Configuration Register	0x4B

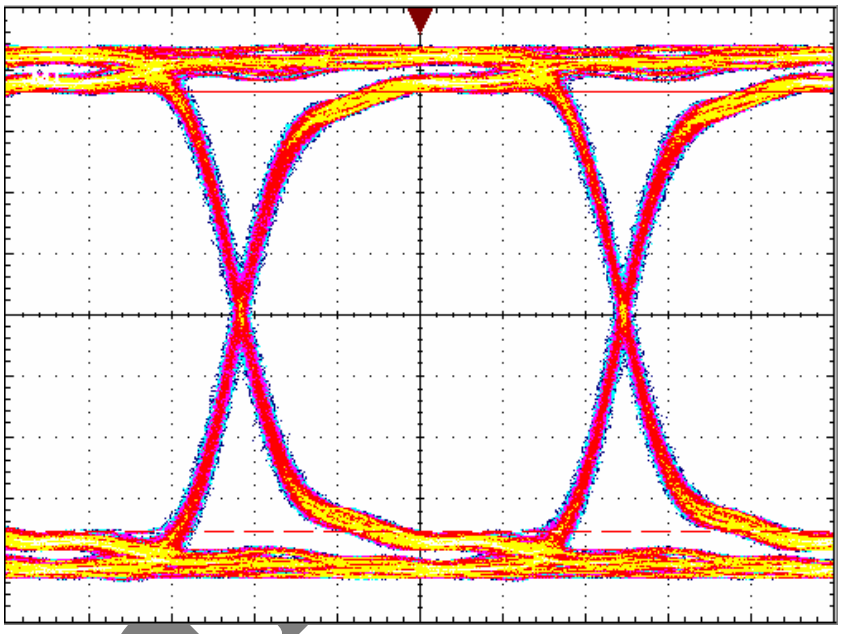
2. Set Polarity Register to Normal

Bus Address	0x05
Command Byte	0x02
Configuration Register	0x00

Eye Diagrams

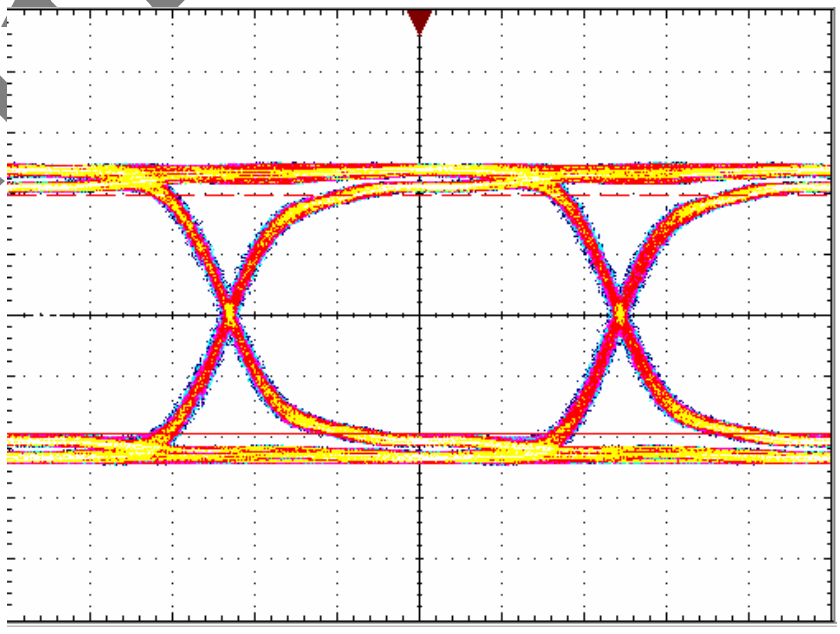
4.25Gbps, 0.0 dB, 2^7 PRBS

Parameters	Results	Units
Rail	1096	mV_{pp}
Eye Height	898	mV_{pp}
Jitter	13	ps
Rise (20-80)	79	ps
Fall (20-80)	80	ps



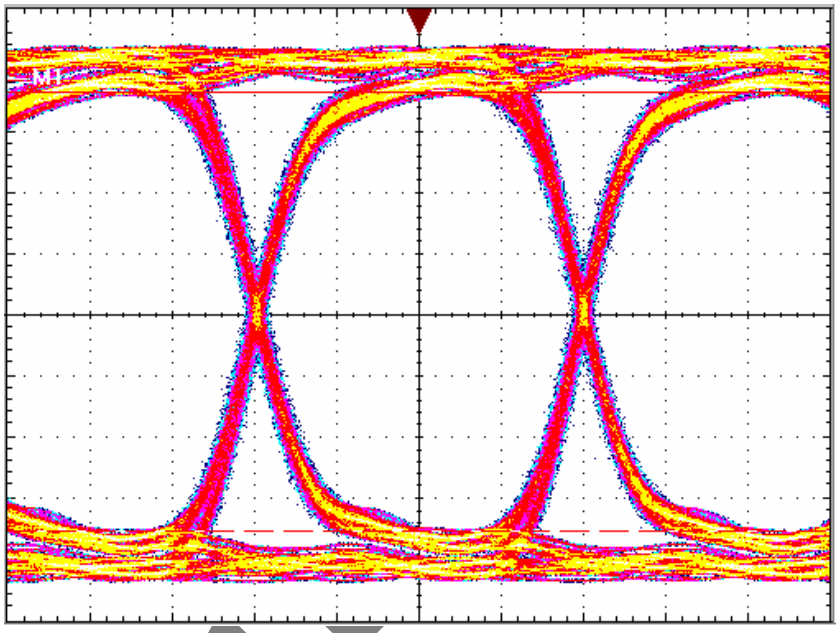
4.25Gbps, 5.0 dB, 2^7 PRBS

Parameters	Results	Units
Rail	619	mV_{pp}
Eye Height	490	mV_{pp}
Jitter	13	ps
Rise (20-80)	80	ps
Fall (20-80)	81	ps



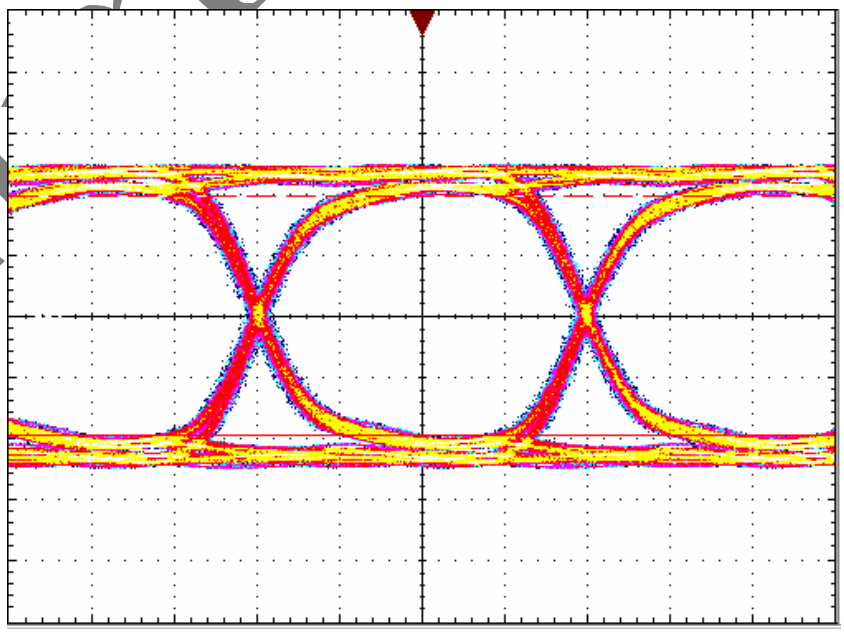
5.0Gbps, 0.0 dB, 2^7 PRBS

Parameters	Results	Units
Rail	1100	mV_{pp}
Eye Height	899	mV_{pp}
Jitter	14	ps
Rise (20-80)	78	ps
Fall (20-80)	80	ps



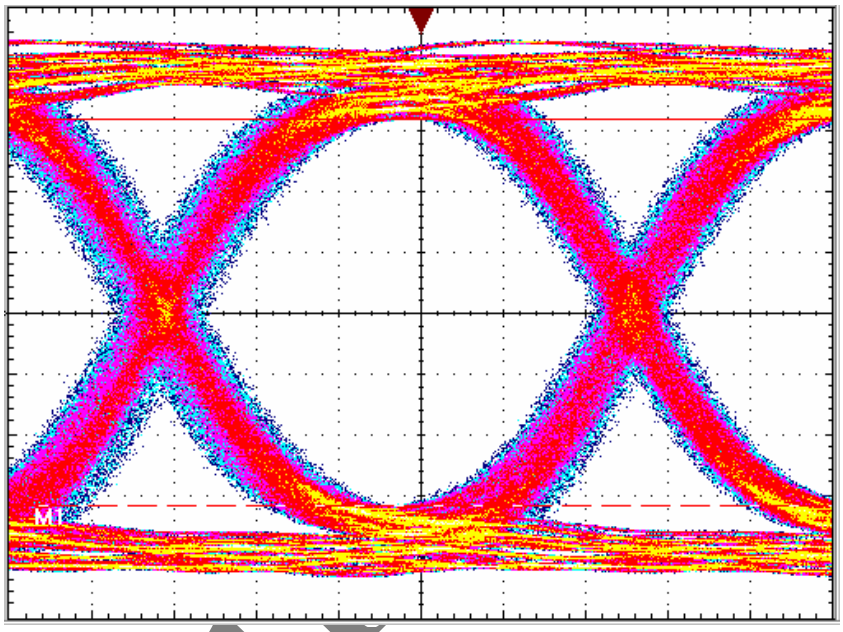
5.0Gbps, 5.0 dB, 2^7 PRBS

Parameters	Results	Units
Rail	622	mV_{pp}
Eye Height	490	mV_{pp}
Jitter	16	ps
Rise (20-80)	81	ps
Fall (20-80)	83	ps



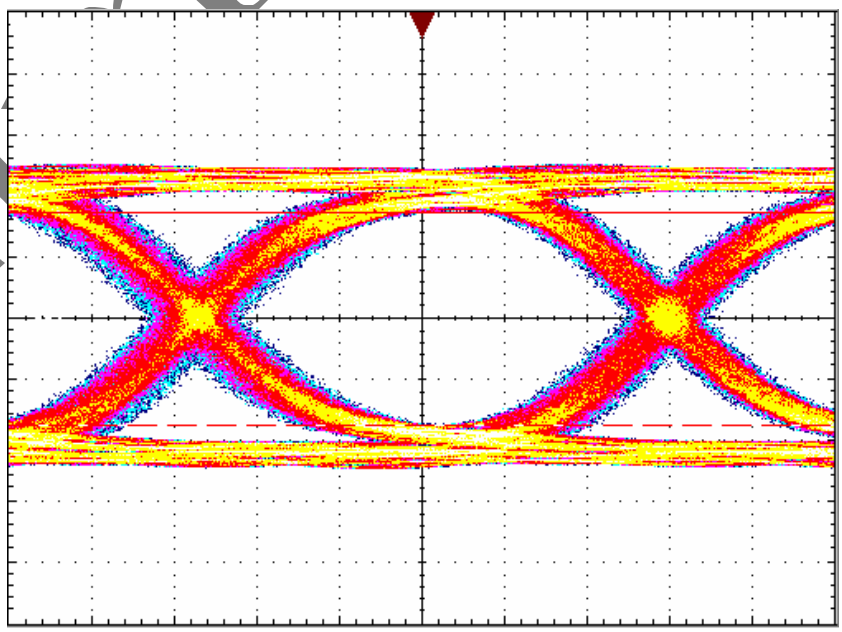
8.75Gbps, 0.0 dB, 2^7 PRBS

Parameters	Results	Units
Rail	1100	mV_{pp}
Eye Height	794	mV_{pp}
Jitter	25	ps
Rise (20-80)	65	ps
Fall (20-80)	66	ps



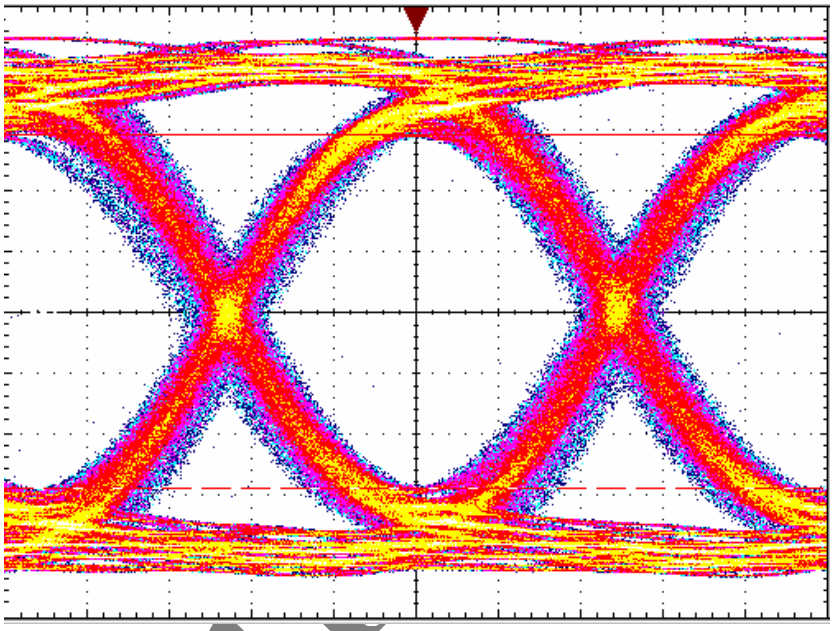
8.75Gbps, 5.0 dB, 2^7 PRBS

Parameters	Results	Units
Rail	619	mV_{pp}
Eye Height	436	mV_{pp}
Jitter	25	ps
Rise (20-80)	66	ps
Fall (20-80)	67	ps



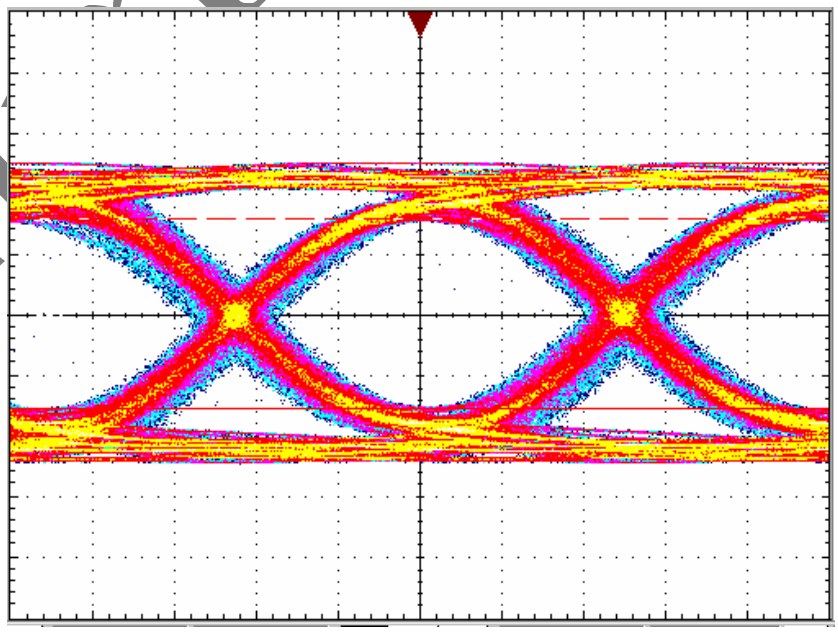
10.3Gbps, 0.0 dB, 2^7 PRBS

Parameters	Results	Units
Rail	1106	mV_{pp}
Eye Height	726	mV_{pp}
Jitter	24	ps
Rise (20-80)	65	ps
Fall (20-80)	64	ps

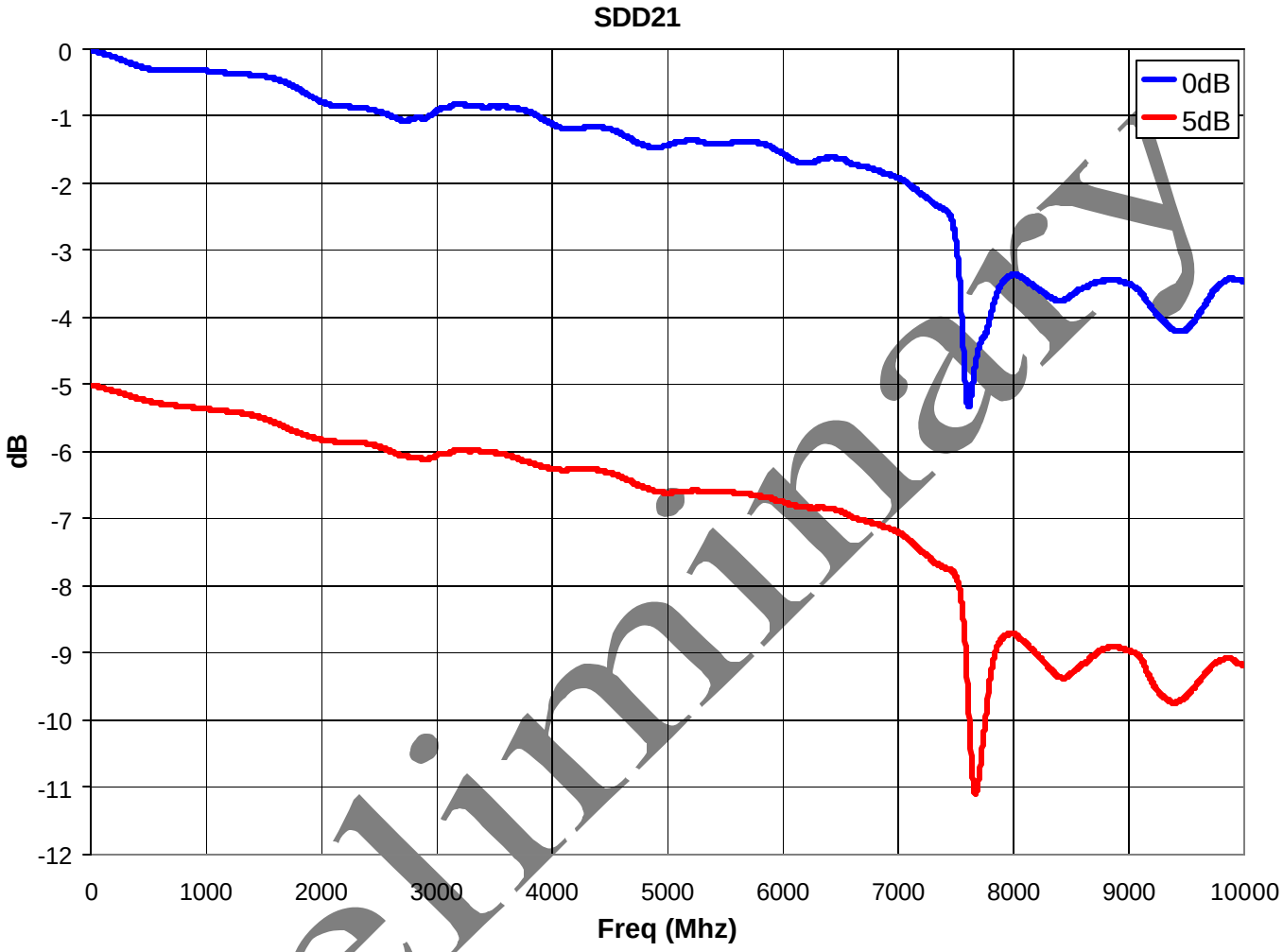


10.3Gbps, 5.0 dB, 2^7 PRBS

Parameters	Results	Units
Rail	622	mV_{pp}
Eye Height	392	mV_{pp}
Jitter	26	ps
Rise (20-80)	64	ps
Fall (20-80)	63	ps

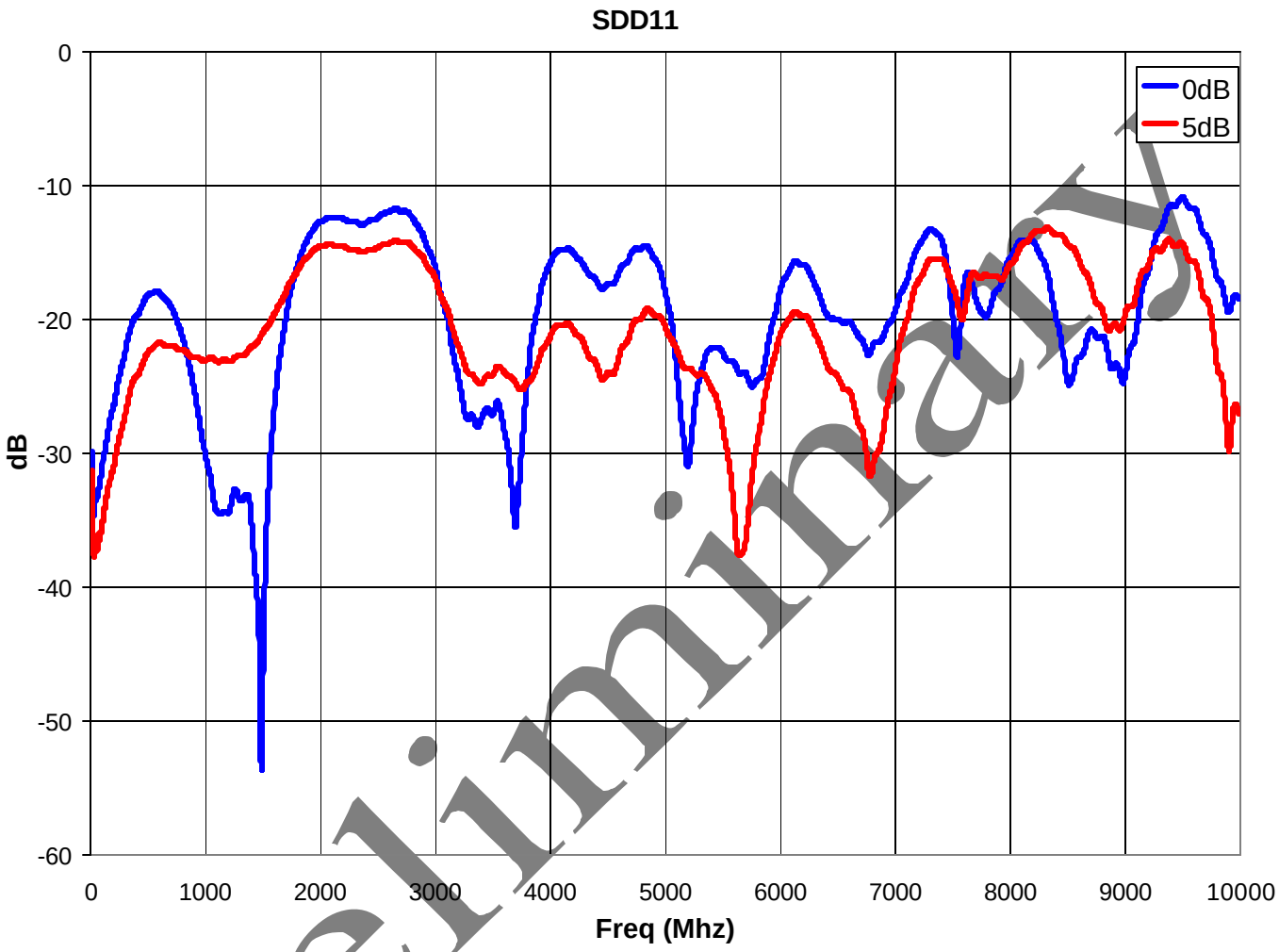


Insertion Loss – SDD21

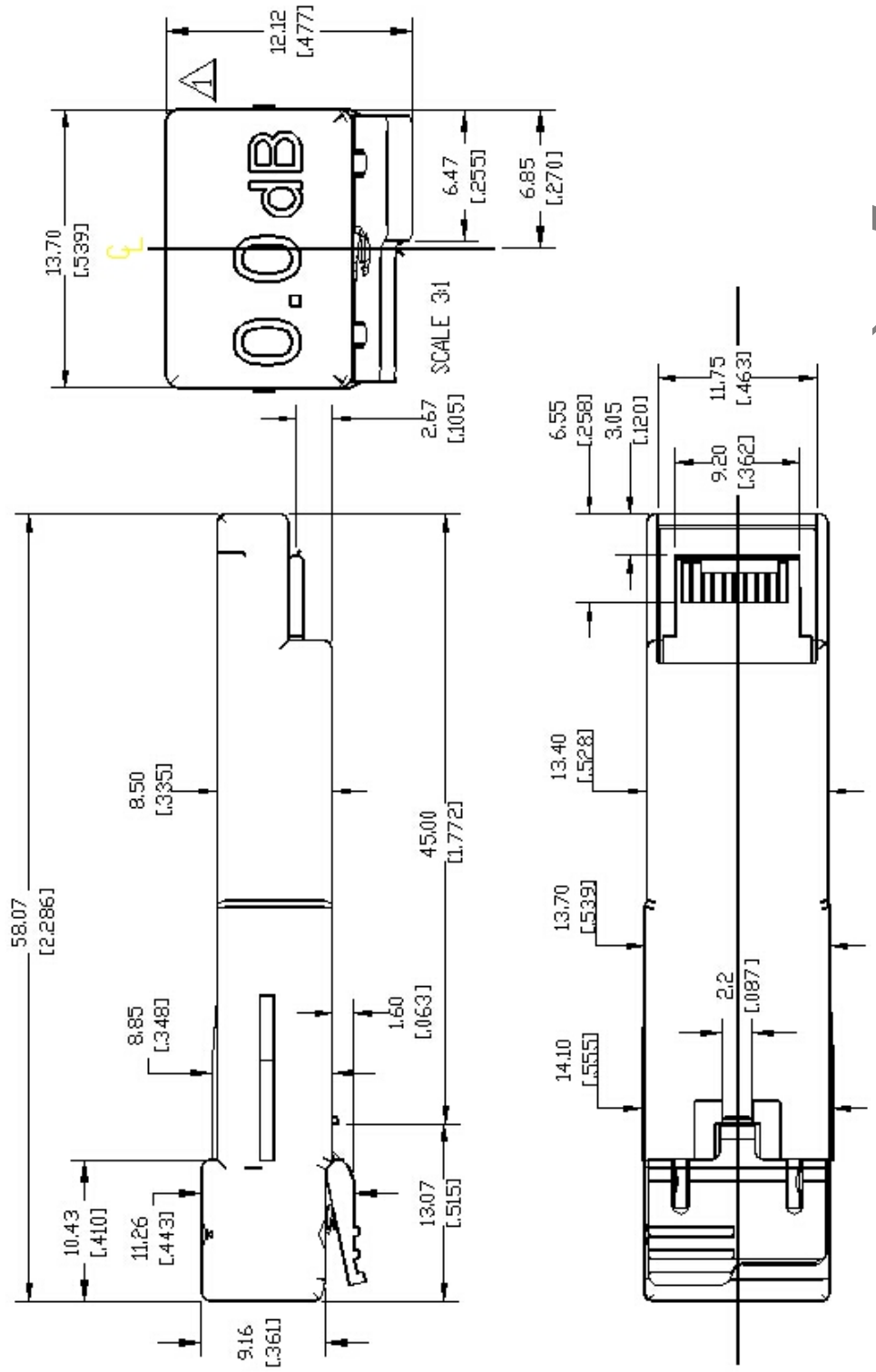


**The 7,750 MHz insertion loss dips are due to the test fixture.

Return Loss – SDD11



Module Dimensions



SFP+ Serial ID (Addresses 0 – 127)

Address	Hex	ASCII
0	03	SFP+
1	04	Serial ID
2	80	Vendor
3	01	Passive – IB
4	00	
5	00	
6	04	1000Base-CX
7	41	Link Lengths
8	84	Cu Passive
9	80	Twin Axial Pair
10	D5	12 to 1 Mbps
11	00	Unspecified
12	78	12000/100
13	00	
14	00	
15	00	
16	00	
17	00	
18	00	Cable Length
19	00	
20	4D	M
21	6F	o
22	6C	l
23	65	e
24	78	x
25	20	
26	49	I
27	6E	n
28	63	c
29	2E	.
30	20	
31	20	
32	20	
33	20	
34	20	
35	20	
36	00	
37	00	Vendor OUI
38	09	
39	3A	

Address	Hex	ASCII
40	37	7
41	34	4
42	37	7
43	36	6
44	35	5
45	2D	-
46	30	0
47	30	0
48	30	0
49	31	1
50	20	
51	20	
52	20	
53	20	
54	20	
55	20	
56	41	Rev A
57	20	
58	20	
59	20	
60	00	
61	00	
62	00	
63	xx	CC Base *
64	00	
65	00	No Options
66	00	
67	00	
68	35	Y
69	31	J
70	32	U
71	33	L
72	34	T
73	30	X
74	30	X
75	33	X
76	32	X
77	20	
78	20	
79	20	
80	20	
81	20	
82	20	
83	20	

Address	Hex	ASCII
84	30	Y
85	32	Y
86	30	M
87	31	M
88	30	D
89	33	D
90	00	
91	00	
92	00	
93	00	
94	00	
95	xx	CC Extended *
96	00	
97	00	
98	00	
99	00	
100	00	
101	00	
102	00	
103	00	
104	00	
105	00	
106	00	
107	00	
108	00	
109	00	
110	00	
111	00	
112	00	
113	00	
114	00	
115	00	
116	00	
117	00	
118	00	
119	00	
120	00	
121	00	
122	00	
123	00	
124	00	
125	00	
126	00	
127	00	

* Checksum calculated during programming.

SFP+ Serial ID (Addresses 128 – 255)

Address	Hex	ASCII
128	00	
129	00	
130	00	
131	00	
132	00	
133	00	
134	00	
135	00	
136	00	
137	00	
138	00	
139	00	
140	00	
141	00	
142	00	
143	00	
144	00	
145	00	
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147	00	
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162	00	
163	00	
164	00	
165	00	
166	00	
167	00	
168	00	
169	00	
170	00	
171	00	

Address	Hex	ASCII
172	00	
173	00	
174	00	
175	00	
176	00	
177	00	
178	00	
179	00	
180	00	
181	00	
182	00	
183	00	
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206	00	
207	00	
208	00	
209	00	
210	00	
211	00	
212	00	
213	00	
214	00	
215	00	

Address	Hex	ASCII
216	00	
217	00	
218	00	
219	00	
220	00	
221	00	
222	00	
223	00	
224	00	
225	00	
226	00	
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247	00	
248	00	
249	00	
250	00	
251	00	
252	00	
253	00	
254	00	
255	00	

* Checksum calculated during programming.